

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1, 3-17, 19-63, and 65-66 are pending in the application, with claims 1, 17, 61-63, and 65-66 being the independent claims. Claims 3-16, 17, 20, 24, 28-30, 42-51, 56, and 58-60 are amended herein to correct informalities. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Claim Objections

Claims 3-16, 43-50, 59, and 60 stand objected to due to informalities in the naming of steps in the claims. Claims 3-16, 43-50, 59, and 60 have been amended to correct these informalities, as suggested by the Examiner. Reconsideration and withdrawal of this objection to claims 3-16, 43-50, 59, and 60 is respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 1, 5-6, 11-13, 16-17, 19, 31-32, 37-39, 42, 49-50, and 57-66 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Azadet et al. (EP 1006 697 A2), hereinafter Azadet, in view of Staszewski et al. (US 6,587,529), hereinafter Staszewski. Applicants have carefully considered the Examiner's comments, but, for the reasons set forth herein, respectfully traverse.

Independent claim 1 recites, among other features, "individually adjusting one or more parameters for each of said N ADC paths, including individually adjusting said N sampling signals to reduce phase errors between said received data signal and each of said N sampling signals in said ADC paths".

In rejecting claim 1, the Examiner concedes that Azadet does not teach the feature of "individually adjusting said N sampling signals to reduce phase errors", as recited in claim 1. The Examiner, however, claims that Staszewski teaches this feature by referring to a timing recovery circuit 401 (FIG. 4) in Staszewski, and further asserts that a motivation to combine the teachings of Azadet and Staszewski exists, in order to provide a timing recovery signal to the N ADC sampling signals to reduce phase errors.

Applicants disagree with the Examiner's assertion of a motivation to combine the teachings of Azadet and Staszewski. Applicants note that Azadet does teach a mechanism to provide timing recovery to the sampling signals (referred to as clock signals Φ_1 through Φ_n in Azadet) using offset cancellation circuits 360-1 through 360-N. This timing recovery mechanism does not include individually adjusting the sampling signals as recited in claim 1, and is performed subsequently to and independently from the analog to digital (A/D) conversion step (320-1 through 320-N) in each path. Also note that Azadet teaches performing clock recovery on the incoming clock signal associated with the received data signal (page 3, lines 34-35), which provides a zero-phase restart and is equivalent to the teaching by Staszewski pointed to by the Examiner. Yet, this does not allow Azadet to individually adjust each of the sampling signals as clock signals Φ_1 through Φ_n in Azadet are generated

uniformly equally as $1/N$ -times the incoming clock signal. A modification of Azadet would be needed therefore in order to combine Staszewski to individually adjust each of the clock signals.

As such, given that Azadet already teaches a mechanism to provide timing recovery, a motivation to combine the alleged teaching of Staszewski and the teachings of Azadet to specifically provide timing recovery in Azadet, as asserted by the Examiner, is lacking. Accordingly, Applicants submit that a *prima facie* case of obviousness has not been established in rejecting claim 1 because there is no motivation to combine the cited references, and therefore that claim 1 is patentable over Azadet and Staszewski. Reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

Claims 5-6, 11-13, 16, 49, 50, 59, and 60 depend directly or indirectly from claim 1. For at least the reasons provided above with respect to claim 1, claims 5-6, 11-13, 16, 49, 50, 59, and 60 are patentable over Azadet and Staszewski. Reconsideration and withdrawal of the rejection of claims 5-6, 11-13, 16, 49, 50, 59, and 60 is respectfully requested.

Independent claim 17 recites, among other features, " means for individually adjusting one or more parameters for each of said N ADC paths, including means for adjusting each of said N sampling signals to reduce sampling phase errors in said N ADC paths". For at least the reasons provided above with respect to claim 1, claim 17 is patentable over Azadet and Staszewski. Reconsideration and withdrawal of the rejection of claim 17 is respectfully requested.

Claims 19, 31, 32, 37-39, 42, 57, and 58 depend directly or indirectly from claim 17. For at least the reasons provided above with respect to claim 17, claims 19, 31, 32, 37, 39, 42, 57, and 58 are patentable over Azadet and Staszewski. Reconsideration and withdrawal of the rejection of claims 19, 31, 32, 37, 39, 42, 57, and 58 is respectfully requested.

Independent claims 61-62 and 64-65 recite, among other features, "individually adjusting one or more parameters for each of said N ADC paths using said control signals, including individually adjusting at least a sampling phase in each of said N ADC paths to compensate for phase errors between each said N sampling signals and said received data signal". As provided above with respect to claim 1, Azadet and Staszewski do not teach or suggest this feature. Accordingly, claims 61-62 and 64-65 are patentable over Azadet and Staszewski. Reconsideration and withdrawal of the rejection of claims 61-62 and 64-65 is respectfully requested.

Independent claim 63 recites similar features of individually adjusting at least a sampling phase in each of the N ADC paths as recited in claims 61-62 and 64-65. Accordingly, for at least the reasons provided above with respect to claims 61-62 and 64-65, claim 63 is patentable over Azadet and Staszewski. Reconsideration and withdrawal of the rejection of claim 63 is respectfully requested.

Claim 64 was sought to be cancelled without prejudice to or disclaimer of the subject matter therein, in the Amendment and Reply filed by Applicants on April 27, 2006. The rejection of claim 64 herein is therefore moot.

Allowable Subject Matter

Claims 3-4, 7-10, 14-15, 20-30, 33-36, 40-41, 43-48, and 51-56 stand objected to as being dependent upon a rejected base claim, but allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 4, 7-10, 14-15, and 43-48 depend directly or indirectly from claim 1. For at least the reasons provided above with respect to claim 1, claims 3, 4, 7-10, 14-15, and 43-48 are patentable. Reconsideration and withdrawal of the objection to claims 3, 4, 7-10, 14-15, and 43-48 is respectfully requested.

Claims 20-30, 33-36, 40-41, and 51-56 depend directly or indirectly from claim 17. For at least the reasons provided above with respect to claim 17, claims 20-30, 33-36, 40-41, and 51-56 are patentable. Reconsideration and withdrawal of the objection to claims 20-30, 33-36, 40-41, and 51-56 is respectfully requested.

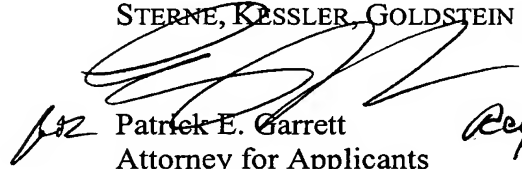
Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is
respectfully requested.

Respectfully submitted,

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